MEM 3012SP

12-BIT SERIAL IN-PARALLEL OUT

DESCRIPTION

The MEM 3012SP is a 12-Bit d.c. serial input parallel output shift register constructed on a single monolithic chip with MOS P-channel enhancement mode transistors. This unit will operate from d.c. to 100 kHz.

MAXIMUM RATINGS

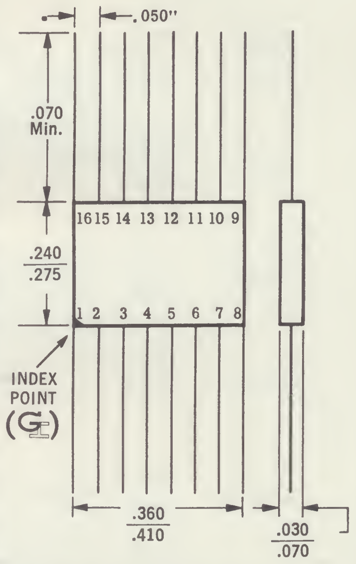
Drain Voltage ($-V_{dd}$) .... −30V to +.3V
Clock and Input Voltages .... −30V to +.3V
Storage Temperature .... −55°C to +150°C
Operating Temperature Range .... −55°C to +85°C

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified):
$V_{dd} = -27$ Volts ±1 Volt, Load = 10MΩ and 10pF.
$T_A = -55°C$ to $+85°C$.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	dc	—	100	kHz	
Clock Pulse Width (ϕ_{pw})	0.4	—	30	μsec.	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	10	μsec.	
Clock & Data Input Logic Levels					
Logic "0"	—	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Clock Fan-In	—	—	3		
Data Input Pulse Width (D_{pw})	0.3	—	—	μsec.	$\phi_{pw} = 0.4$ μsec. SEE FIG. 1
Data Fan-In	—	—	1		
Input Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Output Logic Levels					
Logic "0"	—	−0.5	−1.0	Volt	d.c. to 100 kHz
Logic "1"	−11	−12	—	Volts	
Propagation Delay Plus Fall Time (t_{pd1})	—	—	5.0	μsec.	SEE FIG. 1
Propagation Delay Plus Rise Time (t_{pd2})	—	—	2.0	μsec.	SEE FIG. 1
Fan-Out	—	—	5		
Output Impedance to Ground (Output a Logic "0")	—	—	3000	Ohms	
Supply Current Drain	—	—	6.0	mA	

16 Lead Flatpack

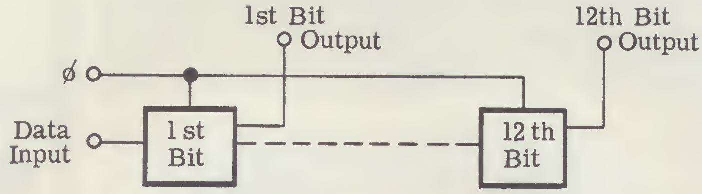


Note: All dimensions in inches.

TERMINALS

P/N	Function
1	Ground
2	Output 6
3	Output 5
4	Output 4
5	Output 3
6	Output 2
7	Output 1
8	Data Input
9	$-V_{dd}$
10	Clock (ϕ)
11	Output 12
12	Output 11
13	Output 10
14	Output 9
15	Output 8
16	Output 7

LOGIC DIAGRAM



TYPICAL TIMING DIAGRAM

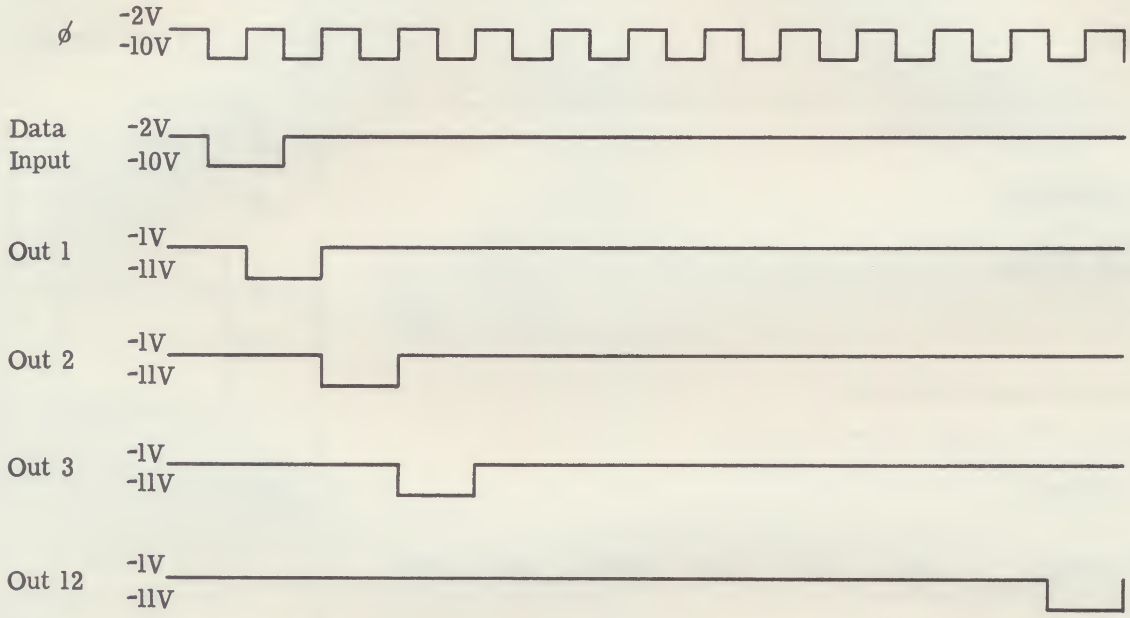
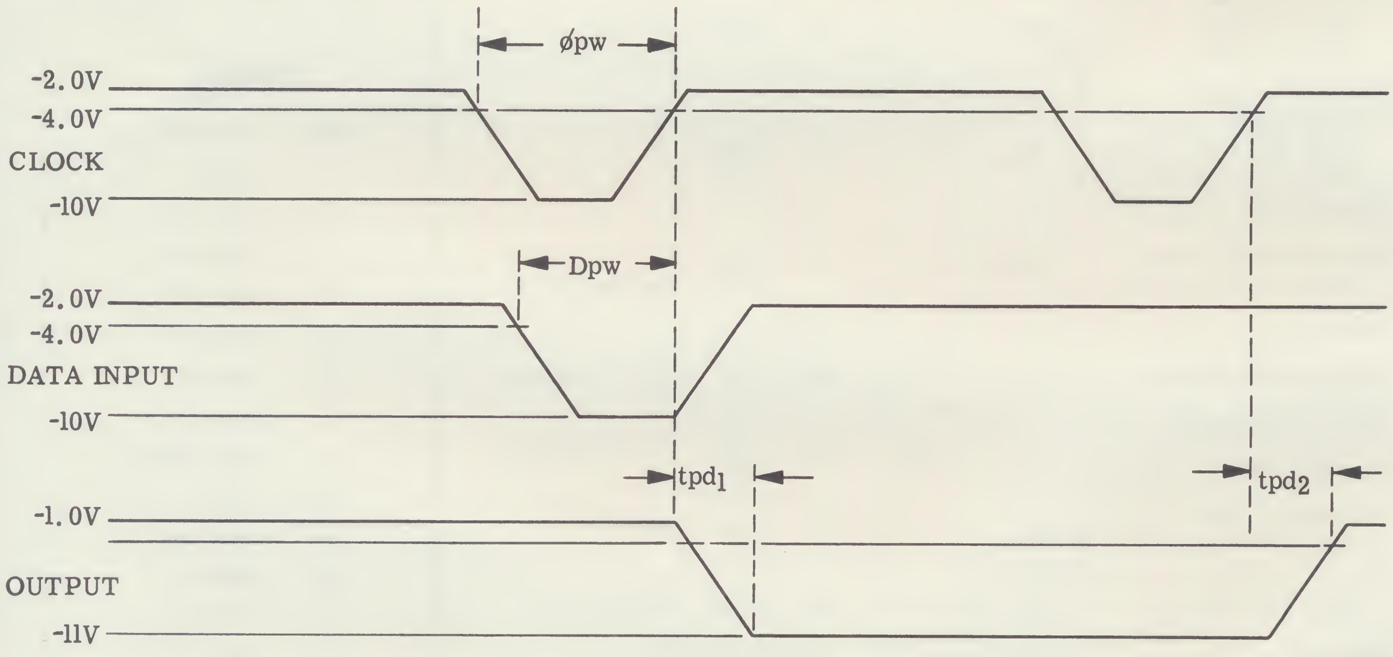


FIGURE 1



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T-6018

GENERAL INSTRUMENT MOS INTEGRATED CIRCUIT

ADVANCE
Sept., 1966

20-BIT SHIFT REGISTER

MEM 3020

20-BIT SHIFT REGISTER

DESCRIPTION

The MEM 3020 is a 20-bit static shift register constructed on a single monolithic chip utilizing MOS P-channel enhancement mode transistors. Each bit of delay has a cross-coupled flip-flop, in order that data might be stored indefinitely between clock pulses. For long term data storage, it is necessary for $\phi2$ to be a logic "1" and $\phi1$ a logic "0". To shift data one bit, $\phi1$ is pulsed momentarily to a logic "1" and $\phi2$ to a logic "0", note that it is important that $\phi1$ and $\phi2$ are not at a logic "1" simultaneously. The output data shall change on the negative edge of the $\phi2$ clock pulse.

MAXIMUM RATINGS

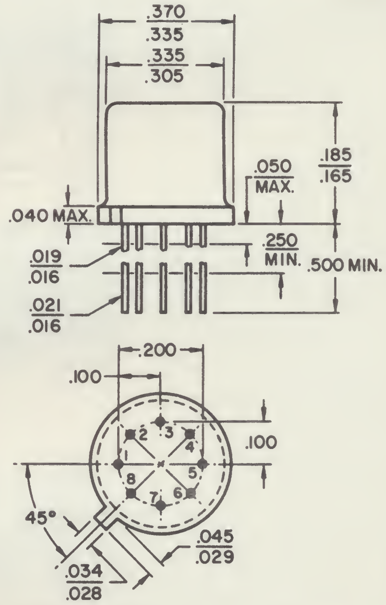
Drain Voltage ($-V_{DD}$)	-30 Volts to $+0.3$ Volt
Gate Voltage ($-V_{GG}$)	-30 Volts to $+0.3$ Volt
Clock and Data Input Voltages	-30 Volts to $+0.3$ Volt
Storage Temperature	-55°C to $+150$°C
Operating Temperature Range	-55°C to $+85$°C

ELECTRICAL CHARACTERISTICS

A. Standard Conditions (unless otherwise specified)
$V_{DD} = -13$ Volts ±1 Volt, $V_{GG} = -27$ Volts ±1 Volt,
Load $= 10$ MΩ and 10 pF., $T_A = -55$°C to $+85$°C.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	d.c.	—	1.0	Mc/s	
Clock Pulse Widths					
$\phi1_{pw}$	0.4	—	10	μs	SEE FIGURE 1
$\phi2_{pw}$	0.4	—	—	μs	SEE FIGURE 1
Clock Delay (ϕd)	0.1	—	10	μs	SEE FIGURE 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	5.0	μs	
Clock Pulse Logic Levels ($\phi1$ & $\phi2$)					
Logic "0"	—	—	-2.0	Volts	
Logic "1"	-26	—	-28	Volts	
Clock Pulse Input Capacitance ($\phi1$ & $\phi2$)	—	4.0	6.0	pF	$\phi1 = \phi2 = 0$ Volts
Data Pulse Width (D_{pw})	0.4	—	—	μs	SEE FIGURE 1
Data Input Capacitance	—	2.0	3.0	pF	$V_{IN} = 0$ Volts
Data Input Logic Levels					
Logic "0"	—	—	-2.0	Volts	
Logic "1"	-10	—	—	Volts	
Data Fan-in	—	—	1.0		
Data Input Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Clock Input Leakage Current	—	—	100	μA	$\phi1 - \phi2 = -26$ Volts
Clock ($\phi2$) Input Impedance	60	—	—	KΩ	$\phi1 = -26$ Volts $\phi2 = 0$ Volts
Output Logic Levels					
Logic "0"	—	0.5	1.0	Volt	d.c.
Logic "1"	-11	-12	—	Volts	d.c.
Fan-Out	—	—	5.0		
Output Impedance to Ground	—	2.0	3.0	KΩ	Output a Logic "0"
Output Drive Capability	-10	-11	—	Volts	$R_L = 17$ KΩ
Output Drive Capability	-5.0	—	—	Volts	$R_L = 2$ KΩ
Supply Current Drain	—	—	6.0	mA	

TO-78



Bottom view
NOTE: All dimensions in inches

TERMINALS

P/N	FUNCTION
1	Output
2	Input
3	Ground
4	Gate Voltage ($-V_{GG}$)
5	Clock ($\phi1$)
6	No Connection
7	Clock ($\phi2$)
8	Drain Voltage ($-V_{DD}$)

MEM 3020

TYPICAL TIMING DIAGRAM

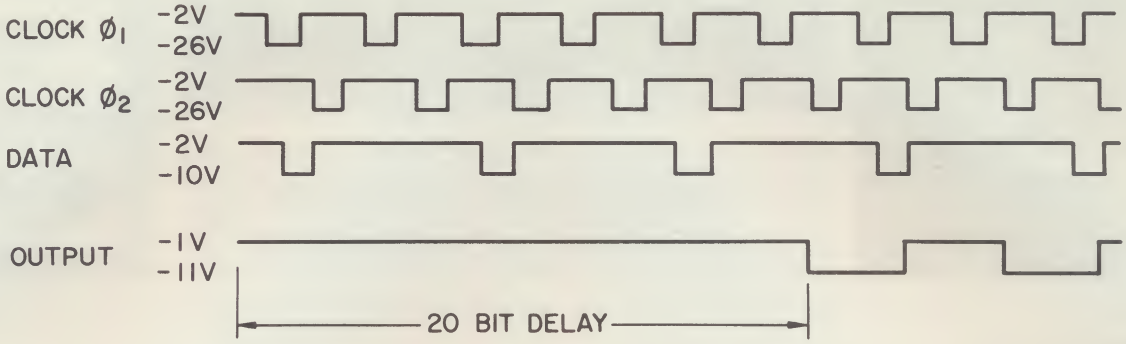
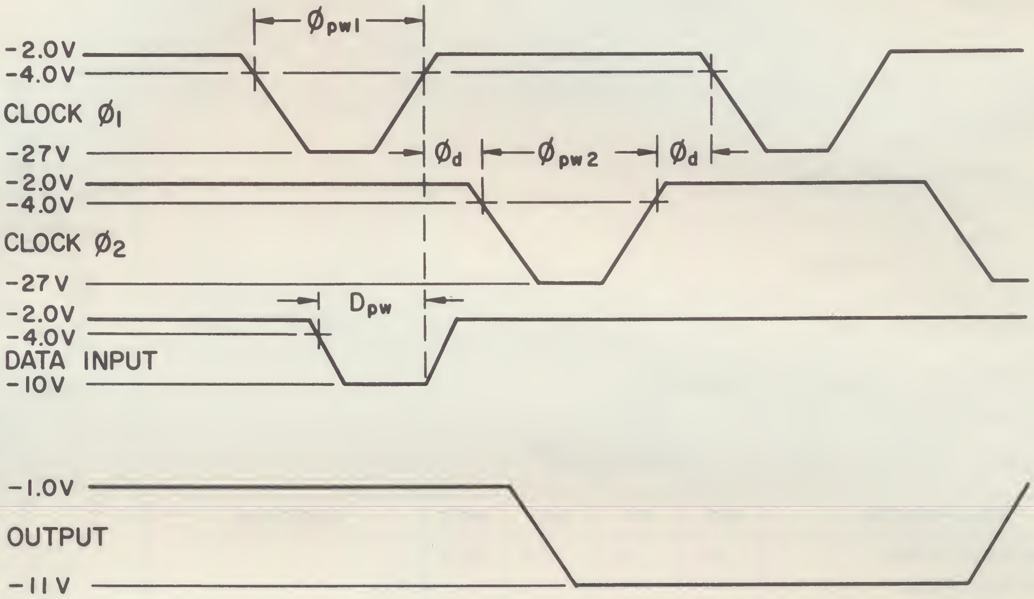
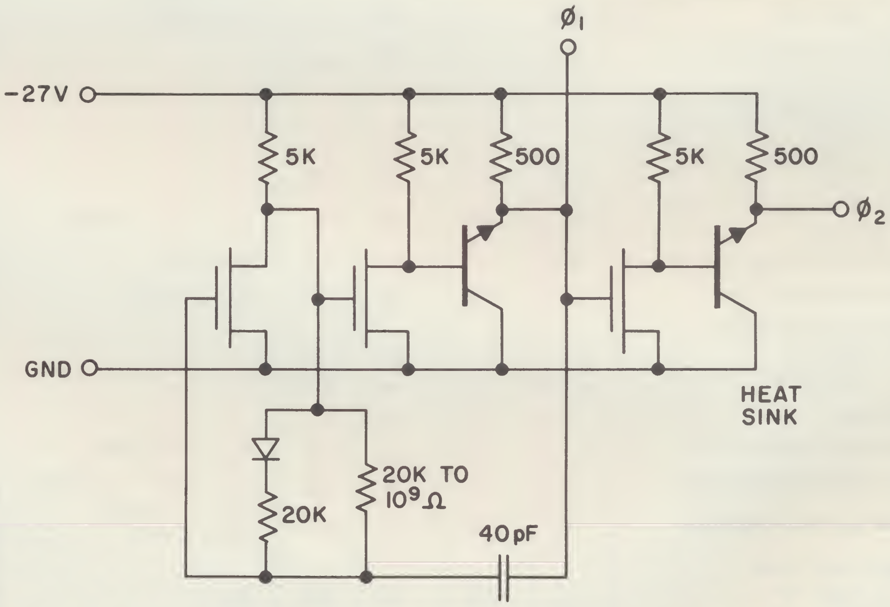


FIGURE 1



APPLICATIONS

Suitable circuit for supplying the clock pulses $\phi 1$ and $\phi 2$



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GENERAL INSTRUMENT

GENERAL INSTRUMENT MOS INTEGRATED CIRCUIT

ADVANCE
Sept., 1966

21-BIT SHIFT REGISTER

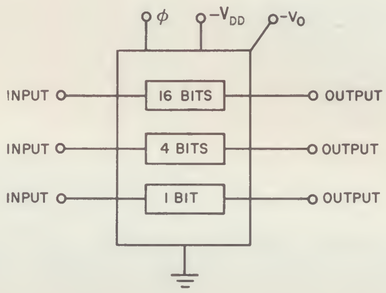
MEM 3021

DESCRIPTION

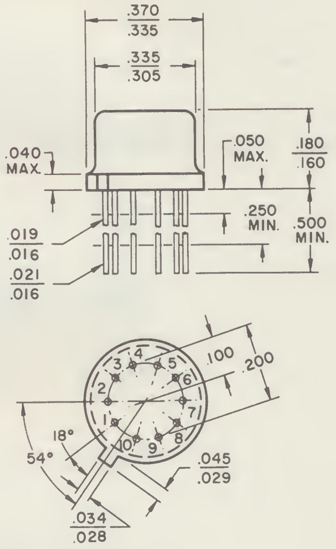
The MEM 3021 is a 1, 4 and 16 bit static shift register constructed on a single monolithic chip utilizing MOS P-channel enhancement mode transistors. Each bit of delay has a cross-coupled flip-flop, in order that data might be stored indefinitely between clock pulses. Only a single phase clock pulse (ϕ) has to be supplied; the additional 180° out of phase clock pulse $(\overline{\phi})$ is generated in the chip.

The outputs will change on the positive edge of the clock pulse. The supply voltage ($-V_O$) for the output stages can have any value between ground and −28 volts. By letting $-V_O$ be just a few volts it is possible to have the shift register drive other types of low voltage NPN transistor logic.

LOGIC DIAGRAM



LOW PROFILE 10 LEAD
TO-74



Bottom view
NOTE: All dimensions in inches

MAXIMUM RATINGS

Drain Voltage	−30 Volts to +.3 Volt
Clock and Input Voltages	−30 Volts to +.3 Volt
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

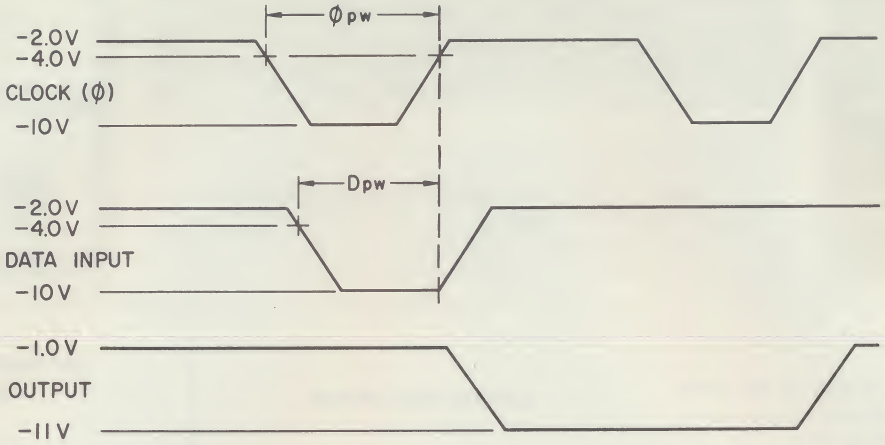
Standard Conditions (unless otherwise specified)
$V_{dd} = V_O = 27$ Volts ±1 Volt, Load = 10MΩ and 10pF. $T_A = -55°C$ to $+85°C$

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	dc	—	500	kHz	
Clock Pulse Width (ϕ_{pw})	1.0	—	10	μsec	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	4.0	μsec	
Clock Input Capacitance	—	—	6.0	pF	$V_{in} = 0$ Volts
Clock & Data Input Logic Levels Logic "0" Logic "1"	 — −10	 — —	 −2.0 —	 Volts Volts	
Data Input Pulse Width (D_{pw})	1.0	—	—	μsec	SEE FIG. 1 $\phi_{pw} = 1.0\ \mu$sec
Data Fan-In	—	—	1.0		
Clock & Data Input Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Output Logic Levels Logic "0" Logic "1"	 — −11	 −0.5 −12	 −1.0 —	 Volt Volts	ϕ = dc to 500 kHz
Fan-Out	—	—	5.0		
Output Impedance to Ground	—	—	5.0	KΩ	(output A Logic "0")
Output Drive Capability	−10	−11	—	Volts	R_L = 17K Ohms
Output Drive Capability	−5.0	—	—	Volts	R_L = 4K Ohms
Supply Current Drain	—	—	5.4	mA	

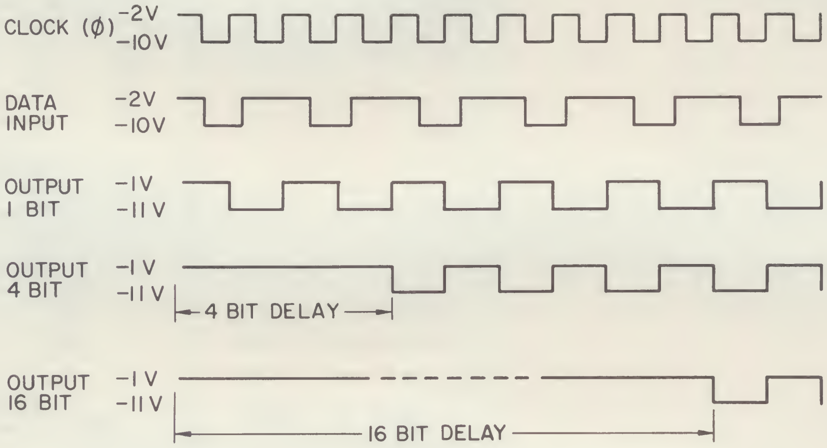
TERMINALS

P/N	Function
1	Input (16 Bit)
2	Clock (ϕ)
3	Output Supply Voltage ($-V_O$)
4	Output (16 Bit)
5	Ground
6	Output (4 Bit)
7	Output (1 Bit)
8	Input (1 Bit)
9	Input (4 Bit)
10	Drain Voltage ($-V_{dd}$)

FIGURE 1

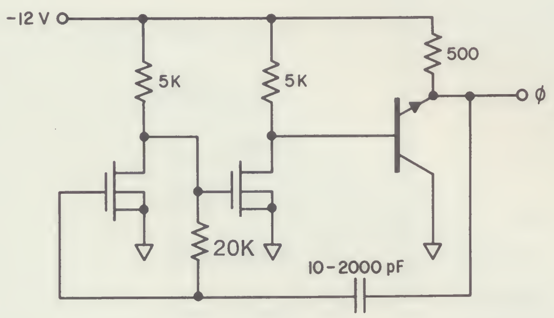


TYPICAL TIMING DIAGRAM

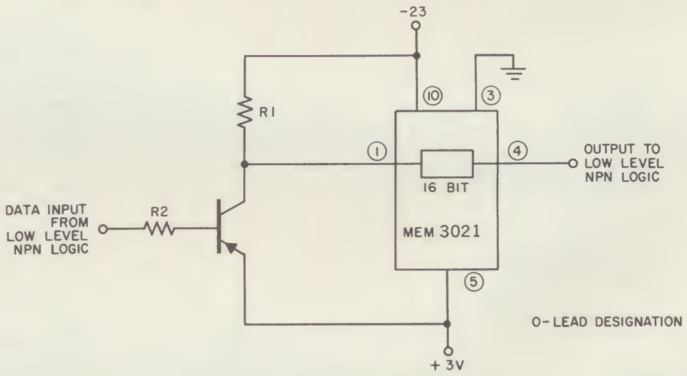


APPLICATIONS

The shift pulse can be supplied from a clock generator as shown below. The shift pulse amplitude requirement is the same as the logic swing required.



The shift register may be interfaced with low level NPN transistor logic, if desired, by using the circuit below.



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GENERAL INSTRUMENT

GENERAL INSTRUMENT MOS INTEGRATED CIRCUIT

ADVANCE
Sept., 1966

21-BIT SHIFT REGISTER

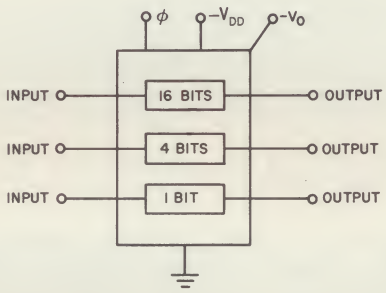
MEM 3021B

DESCRIPTION

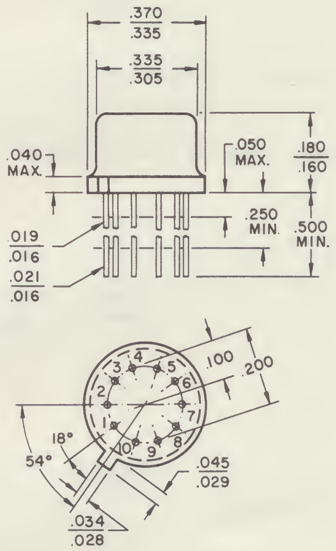
The MEM 3021B is a 1, 4 and 16 bit static shift register constructed on a single monolithic chip utilizing MOS P-channel enhancement mode transistors. Each bit of delay has a cross-coupled flip-flop, in order that data might be stored indefinitely between clock pulses. Only a single phase clock pulse (ϕ) has to be supplied; the additional 180° out of phase clock pulse $(\overline{\phi})$ is generated in the chip.

The outputs will change on the positive edge of the clock pulse. The supply voltage ($-V_O$) for the output stages can have any value between ground and -28 volts. By letting $-V_O$ be just a few volts it is possible to have the shift register drive other types of low voltage NPN transistor logic.

LOGIC DIAGRAM



LOW PROFILE 10 LEAD TO-74



Bottom view
NOTE: All dimensions in inches

MAXIMUM RATINGS

Drain Voltage	−30 Volts to +.3 Volt
Clock and Input Voltages	−30 Volts to +.3 Volt
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

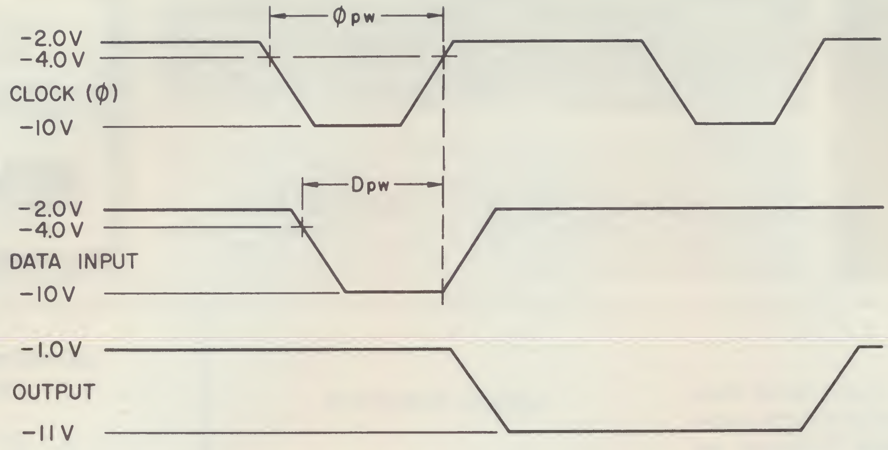
Standard Conditions (unless otherwise specified)
$V_{dd} = V_O = 27$ Volts ± 1 Volt, Load $= 10M\Omega$ and 10pF. $T_A = -55°C$ to $+85°C$

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	dc	—	250	kHz	
Clock Pulse Width (ϕ_{pw})	1.0	—	10	μsec	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	4.0	μsec	
Clock Input Capacitance	—	—	6.0	pF	$V_{in} = 0$ Volts
Clock & Data Input Logic Levels Logic "0" Logic "1"	 — −10	 — —	 −2.0 —	 Volts Volts	
Data Input Pulse Width (D_{pw})	1.0	—	—	μsec	SEE FIG. 1 $\phi_{pw} = 1.0\ \mu$sec
Data Fan-In	—	—	1.0		
Clock & Data Input Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Output Logic Levels Logic "0" Logic "1"	 — −11	 −0.5 −12	 −1.0 —	 Volt Volts	ϕ = dc to 250 kHz
Fan-Out	—	—	5.0		
Output Impedance to Ground	—	—	5.0	KΩ	(output A Logic "0")
Output Drive Capability	−10	−11	—	Volts	$R_L = 17K$ Ohms
Output Drive Capability	−5.0	—	—	Volts	$R_L = 4K$ Ohms
Supply Current Drain	—	—	5.4	mA	

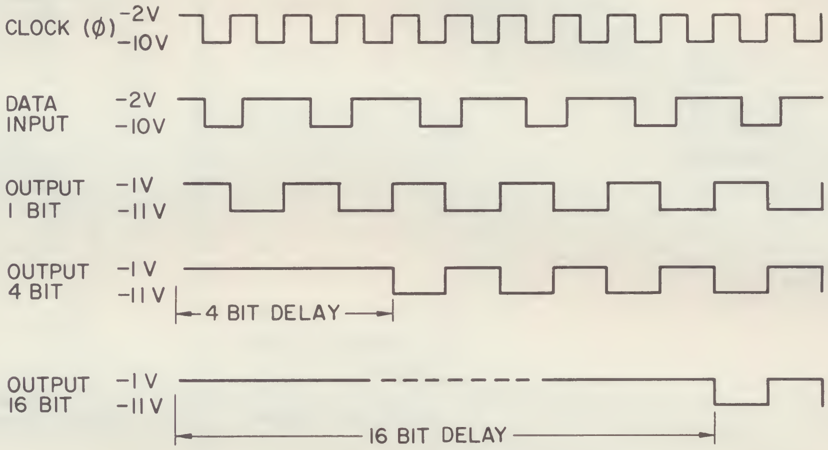
TERMINALS

P/N	Function
1	Input (16 Bit)
2	Clock (ϕ)
3	Output Supply Voltage ($-V_O$)
4	Output (16 Bit)
5	Ground
6	Output (4 Bit)
7	Output (1 Bit)
8	Input (1 Bit)
9	Input (4 Bit)
10	Drain Voltage ($-V_{dd}$)

FIGURE 1

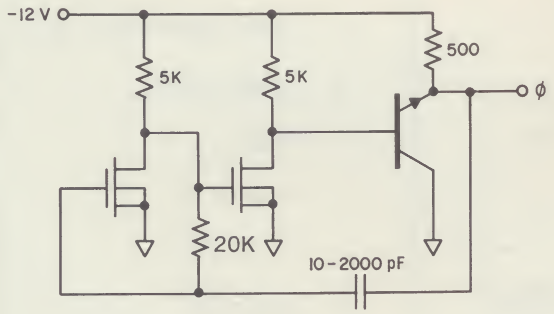


TYPICAL TIMING DIAGRAM

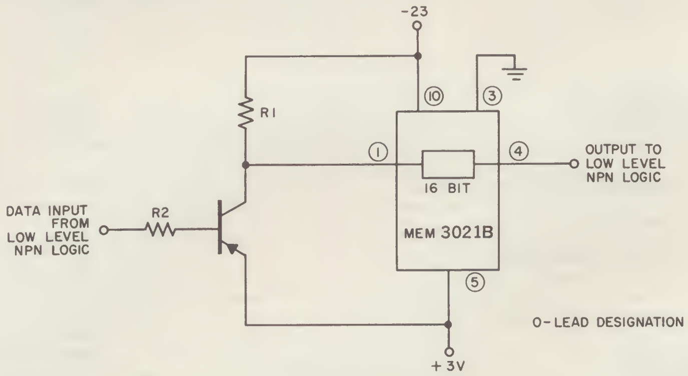


APPLICATIONS

The shift pulse can be supplied from a clock generator as shown below. The shift pulse amplitude requirement is the same as the logic swing required.



The shift register may be interfaced with low level NPN transistor logic, if desired, by using the circuit below.



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GENERAL INSTRUMENT
MOS INTEGRATED CIRCUIT

GENERAL INSTRUMENT

ADVANCE
Sept., 1966

DUAL 25-BIT SHIFT REGISTER

MEM 3050

DESCRIPTION

The MEM 3050 is a dual 25-Bit dynamic shift register constructed on a single monolithic chip utilizing MOS P-channel enhancement mode transistors.

MAXIMUM RATINGS

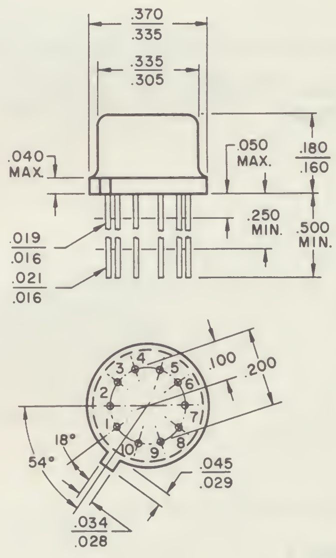
Clock Voltages ($\phi 1$ and $\phi 2$)	−30V to +.3V
Data Input Voltage	−30V to +.3V
Supply Voltage (V_s)	−30V to +.3V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified):
Load = 10MΩ and 10pF.
$V_s = -27$ Volts ±1 Volt, $\phi 1$ and $\phi 2 = -27$ Volts ±1 Volt.
R1 = 20KΩ, $T_A = -55$°C to +85°C.

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Repetition Rate	10	—	—	kHz	$\phi 1_{pw} = 45$ μsec. $\phi 2_{pw} = 45$ μsec.
Clock Repetition Rate	—	—	500	kHz	$\phi 1_{pw} = 0.4$ μsec. $\phi 2_{pw} = 0.4$ μsec.
Clock Pulse Width ($\phi 1_{pw}$ and $\phi 2_{pw}$)	400	—	—	nsec.	SEE FIG. 1
Clock Delay (ϕd)	400	—	—	nsec.	SEE FIG. 1
Clock Logic Levels					
Logic "0"	0	—	−0.5	Volts	
Logic "1"	−26	—	−28	Volts	
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	100	nsec.	$\phi 1_{pw} = 0.4$ μsec. $\phi 2_{pw} = 0.4$ μsec.
Data Input Logic Levels					
Logic "0"	0	—	−2.0	Volts	$\phi 1_{pw} = 0.4$ μsec.
Logic "1"	−11	—	—	Volts	$\phi 2_{pw} = 0.4$ μsec.
Data Pulse Width (D_{pw})	200	—	—	nsec.	$\phi d = 0.4$ μsec. SEE FIG. 1
Output Logic Levels					
Logic "0"	—	—	−1.0	Volt	$\phi 1_{pw} = 0.4$ μsec.
Logic "1"	−14	—	—	Volts	$\phi 2_{pw} = 0.4$ μsec.
Output Fall time ($_{tf}$)	—	—	550	nsec.	$\phi 1_{pw} = 0.4$ μsec. $\phi 2_{pw} = 0.4$ μsec. SEE FIG. 1
Fan-In	—	—	1.0		
Fan-Out	—	—	5.0		
Output Pulse Width (O_{pw})	1.0	—	—	μsec.	$\phi 1_{pw} = 0.4$ μsec. $\phi 2_{pw} = 0.4$ μsec. SEE FIG. 1
Output Impedance to Ground	—	—	1000	Ohms	Output a Logic "0"
Clock Input Leakage Current	—	—	100	μA	$V_{in} = -26$ Volts
Data Input Capacitance	—	4.0	—	pF	$V_{in} = 0$ Volts
Clock Input Capacitance	—	10.0	—	pF	$V_{in} = 0$ Volts

LOW PROFILE 10 LEAD TO-74



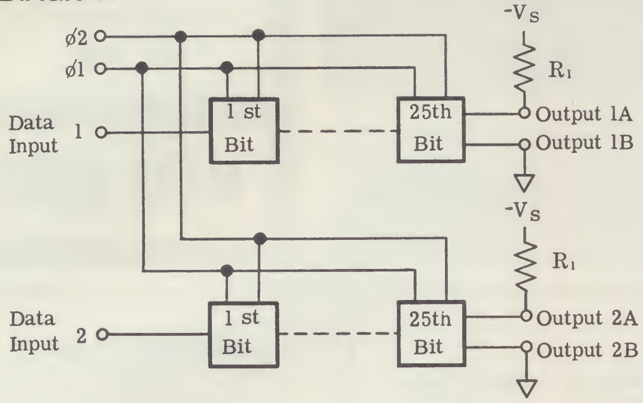
Bottom view
NOTE: All dimensions in inches

TERMINALS

P/N	Function
1	Data Input 1
2	Output 1A
3	Output 1B
4	Clock $\phi 2$
5	Ground
6	Clock $\phi 1$
7	Output 2B
8	Output 2A
9	Data Input 2
10	No Connection

DUAL 25-BIT SHIFT REGISTER
MEM 3050

LOGIC DIAGRAM



NOTE: The output transistor requires an external resistor and a −12 to −27 volt power supply. When connected as shown in the logic diagram, the output of the 25th stage will be inverted with respect to its Data Input. When a non-inverted output is required, Output 1A (or 2A) can be connected to −Vs, and R₁ connected between Output 1B (or 2B) and ground. The output stage will then operate as a non-inverting source follower.

TYPICAL TIMING DIAGRAM

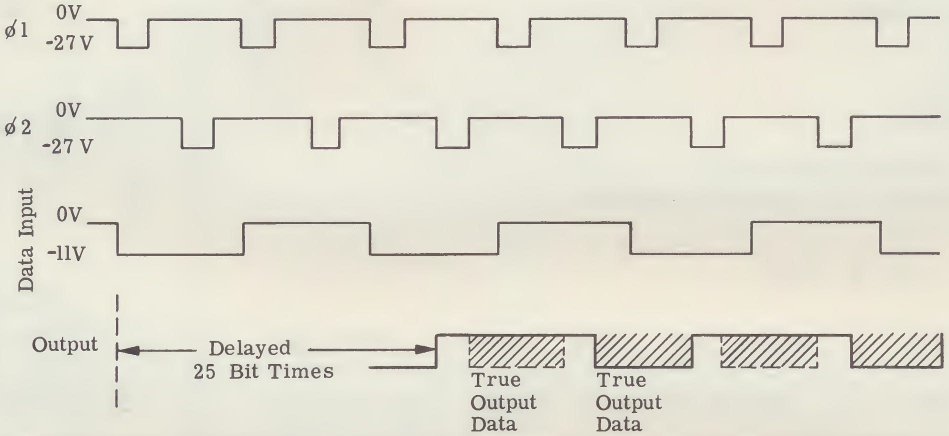
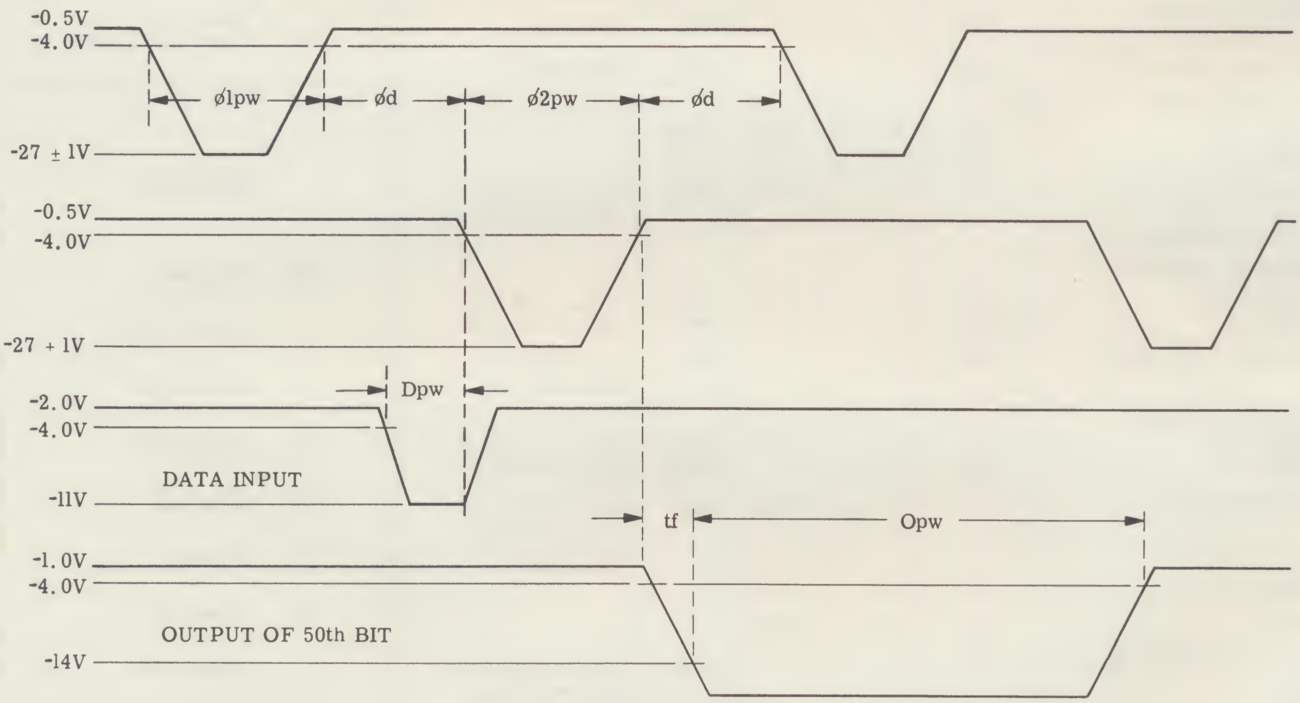


FIGURE 1



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GENERAL INSTRUMENT MOS TRANSISTOR

TECHNICAL SPECIFICATIONS
Sept., 1966

P CHANNEL-ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

2N4353

FEATURES

- 10^{12} ohms input resistance
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

- Very high input impedance amplifiers
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF and IF amplifiers
- Multiplexers
- Analog switches

MAXIMUM RATINGS:

Temperature

Storage Temperature Range, T_{stg} .... −60°C to 125°C

Lead (Terminal) Temperature, 1/16" from the seated surface (or case) for 10 seconds .... 230°C

Voltage at 25°C Free-Air Temperature

Forward Gate-Source Voltage .... −30V

Drain-Source Voltage .... −25V

Drain-Gate Voltage .... −25V

Current

Reverse Gate Current .... +1 mA

Forward Gate Current .... −.01 mA

Drain Current .... −100 mA

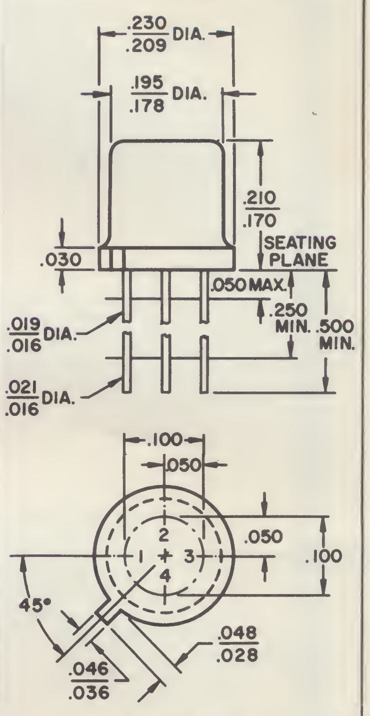
Power

Continuous Device Dissipation at or below 25°C Free-Air Temperature .... 250 mW

Linear Derating Factor .... 2 mW/°C

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$I_{G(f)}$	Gate Forward Current		−1.0	nA	$V_{GS} = -20V$, $V_{DS} = 0V$
$I_{G(f)}$	Gate Forward Current		−100	nA	$V_{GS} = -20V$, $V_{DS} = 0V$, $T_A = 85°C$
$V_{(BR)GSS}$	Gate-Source Reverse Breakdown Voltage		+3.0	V	$I_G = 1$ mA, $V_{DS} = 0V$
$V_{GS(f)}$	Gate-Source Forward Voltage	−30	−60	V	$I_G = -.01$ mA, $V_{DS} = 0V$
$I_{D(on)}$	"ON" Drain Current	−30		mA	$V_{DS} = -10V$, $V_{GS} = -20V$ Pulse Test: 300 μs pw, 2% Duty Cycle
V_{GS}	Gate-Source Voltage	−5.0	−10	V	$V_{DS} = -10V$, $I_D = -10$ mA
$V_{GS(th)}$	Gate-Source Threshold Voltage	−2.5	−5.0	V	$V_{DS} = -10V$, $I_D = -10$ μA
I_{DSS}	Zero-Gate-Voltage Drain Current		−5	nA	$V_{DS} = -10V$, $V_{GS} = 0$ V
$r_{DS(on)}$	Static Drain-Source "ON" Resistance		300	Ohms	$I_D = -0.1$ mA, $V_{GS} = -20V$
Y_{fs}	Transadmittance	1000	4000	μmhos	$V_{DS} = -10V$, $I_D = -10$ mA
Y_{os}	Output Admittance		350	μmhos	1 kHz $V_{DS} = -10V$, $I_D = -10$ mA
C_{ISS}	Input Capacitance		12	pF	1 MHz $V_{DS} = -10V$, $I_D = -10$ mA
C_{RSS}	Reverse Transfer Capacitance		4	pF	1 MHz $V_{DS} = -10V$, $I_D = -10$ mA
C_{DGO}	Drain-Gate Capacitance		4	pF	1 MHz $V_{DG} = -10V$, $I_S = 0$ mA
$R_{e(Yfs)}$	Forward Transconductance	900		μmhos	30 MHz $V_{DS} = -10V$, $I_D = -10$ mA

TO-72



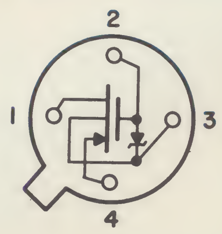
Bottom view
NOTE: All dimensions in inches

TERMINALS

P/N	FUNCTION
1	Drain
2	Gate
3	Body (Case)
4	Source

NOTE: Case Material — Metallic (Electrically Non-insulated)

TERMINAL DIAGRAM

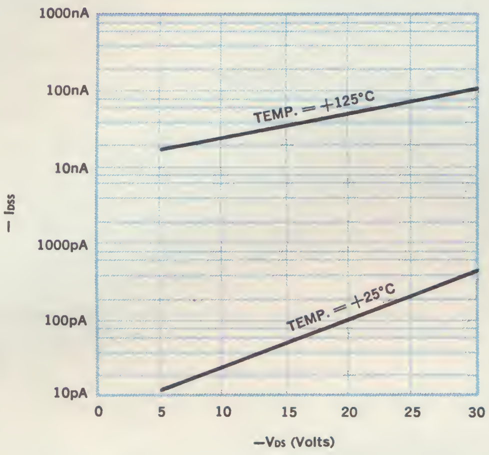


P CHANNEL-ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

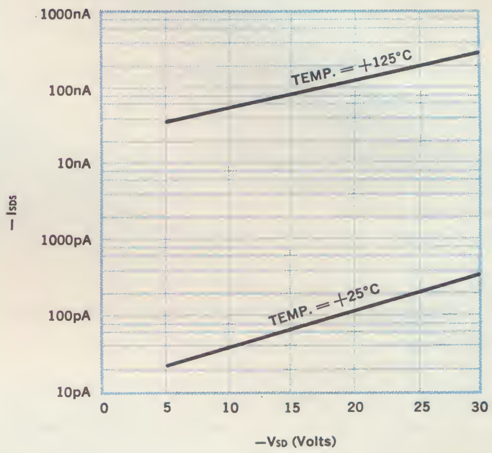
2N4353

TYPICAL ELECTRICAL CHARACTERISTICS

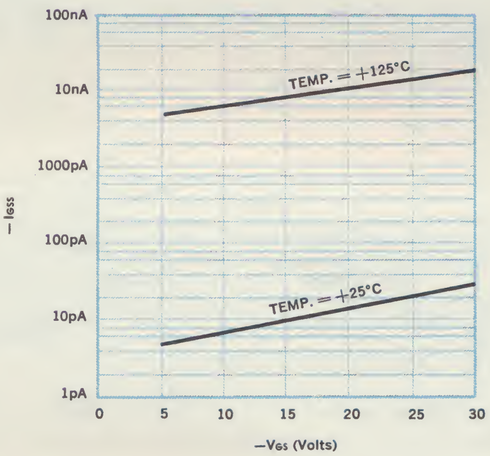
DRAIN LEAKAGE VS DRAIN VOLTAGE



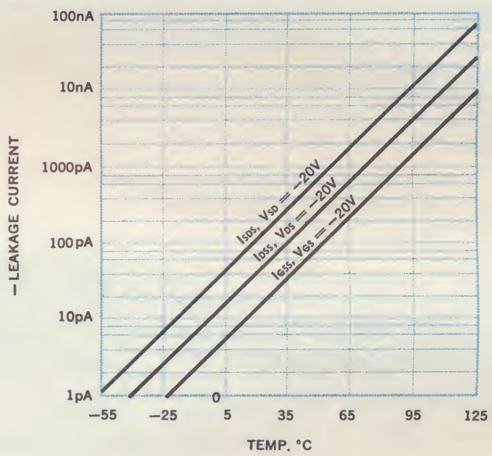
SOURCE LEAKAGE VS SOURCE VOLTAGE



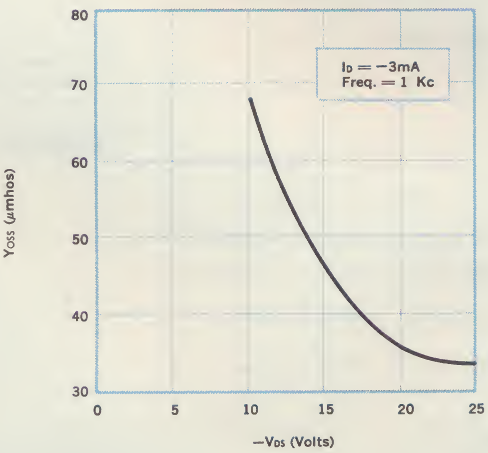
GATE LEAKAGE VS GATE VOLTAGE



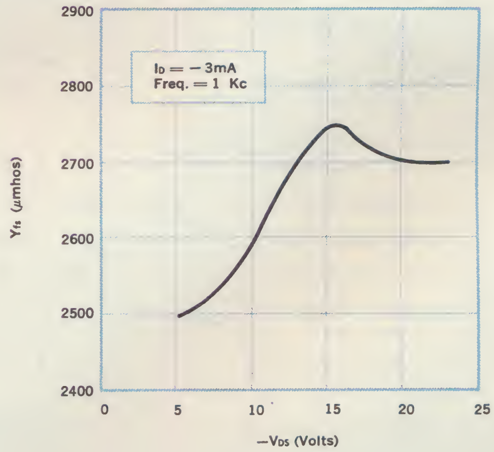
LEAKAGE CURRENT VS TEMPERATURE



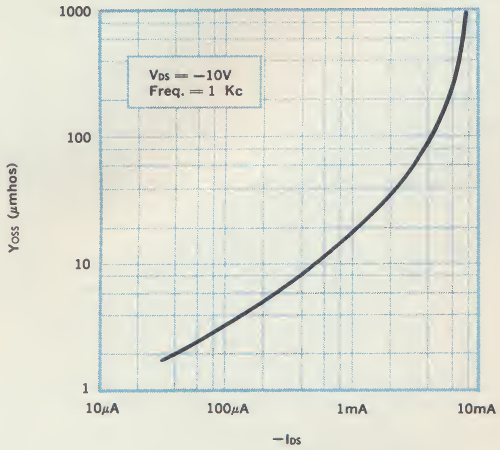
OUTPUT ADMITTANCE VS DRAIN VOLTAGE



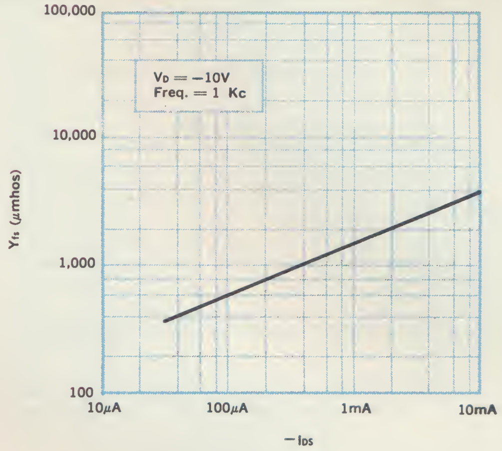
FORWARD TRANSADMITTANCE VS DRAIN VOLTAGE



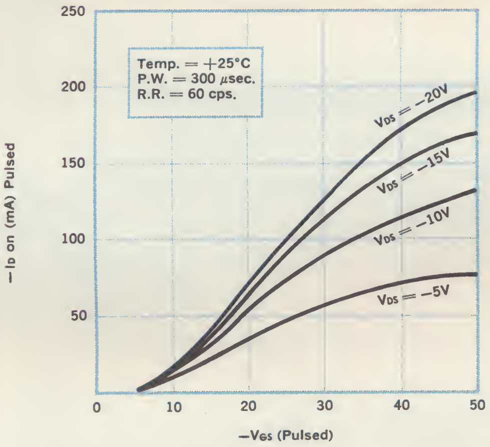
OUTPUT ADMITTANCE VS DRAIN CURRENT



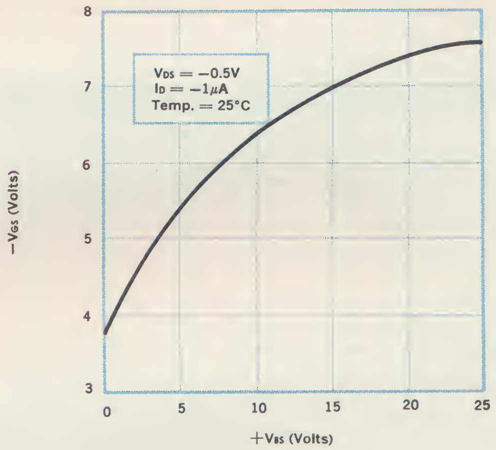
FORWARD TRANSADMITTANCE VS DRAIN CURRENT



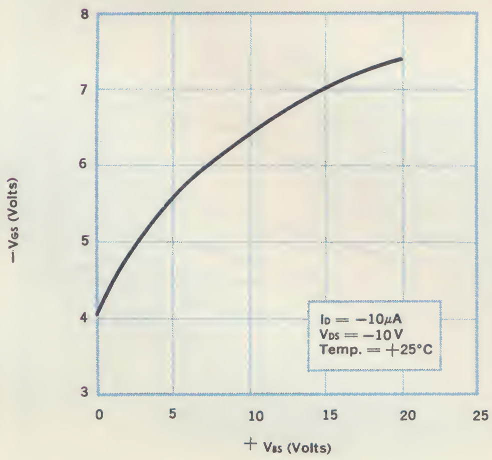
DRAIN CURRENT (PULSED) VS GATE VOLTAGE (PULSED)



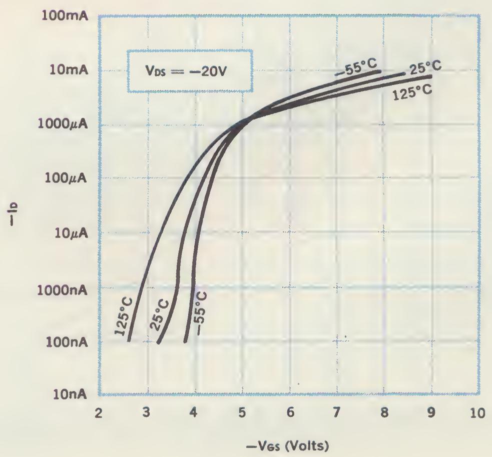
GATE VOLTAGE VS BODY TO SOURCE VOLTAGE



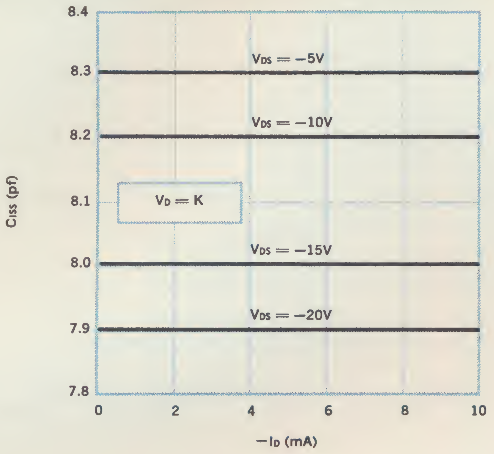
GATE VOLTAGE VS BODY TO SOURCE VOLTAGE



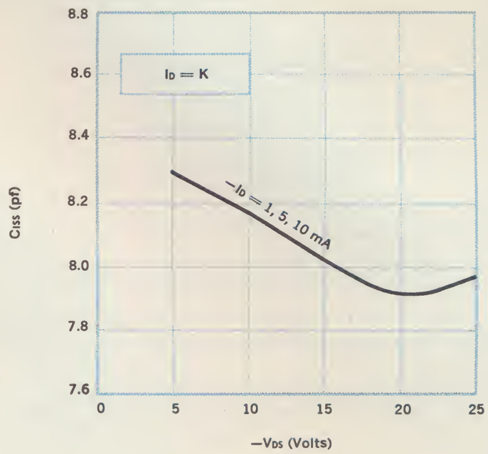
DRAIN CURRENT VS GATE VOLTAGE



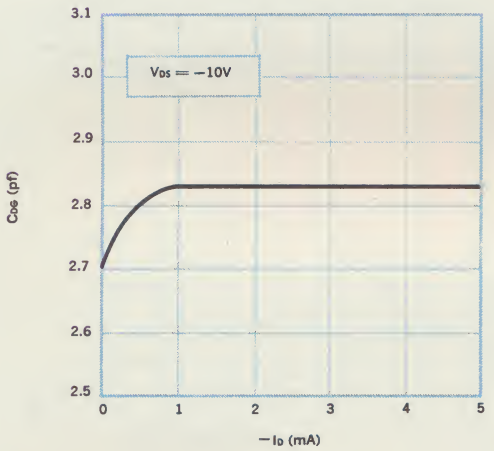
INPUT CAPACITANCE VS DRAIN CURRENT



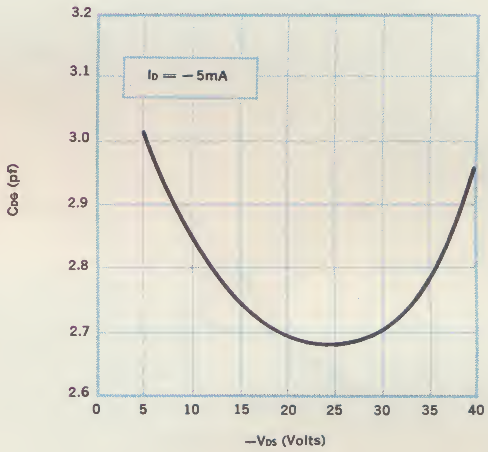
INPUT CAPACITANCE VS DRAIN VOLTAGE



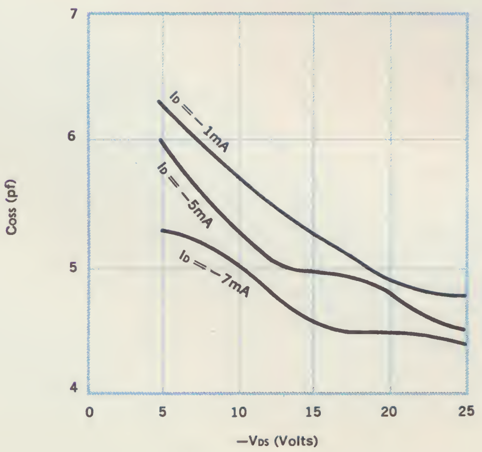
DRAIN TO GATE CAPACITANCE VS DRAIN CURRENT



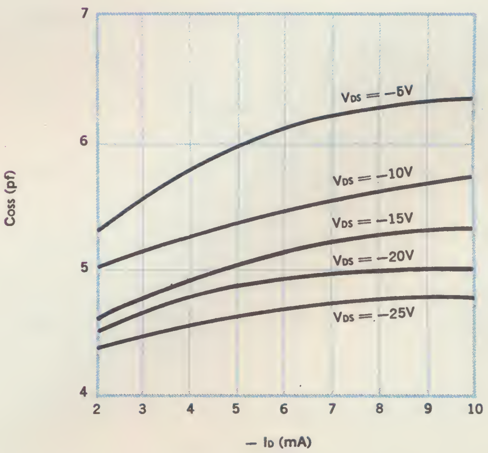
DRAIN TO GATE CAPACITANCE VS DRAIN VOLTAGE



OUTPUT CAPACITANCE VS DRAIN VOLTAGE

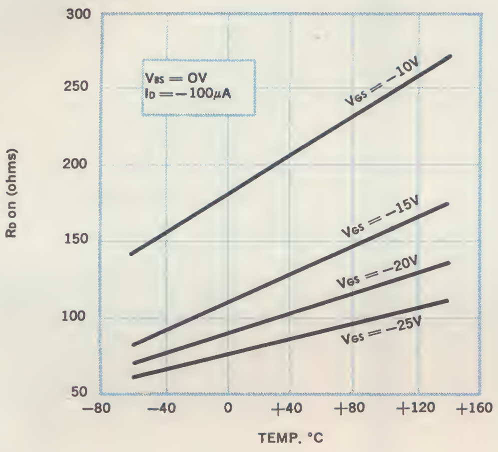


OUTPUT CAPACITANCE VS DRAIN CURRENT

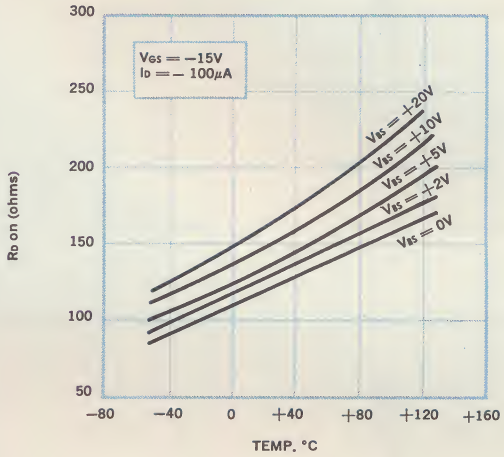


TYPICAL ELECTRICAL CHARACTERISTICS

DYNAMIC DRAIN RESISTANCE VS TEMPERATURE

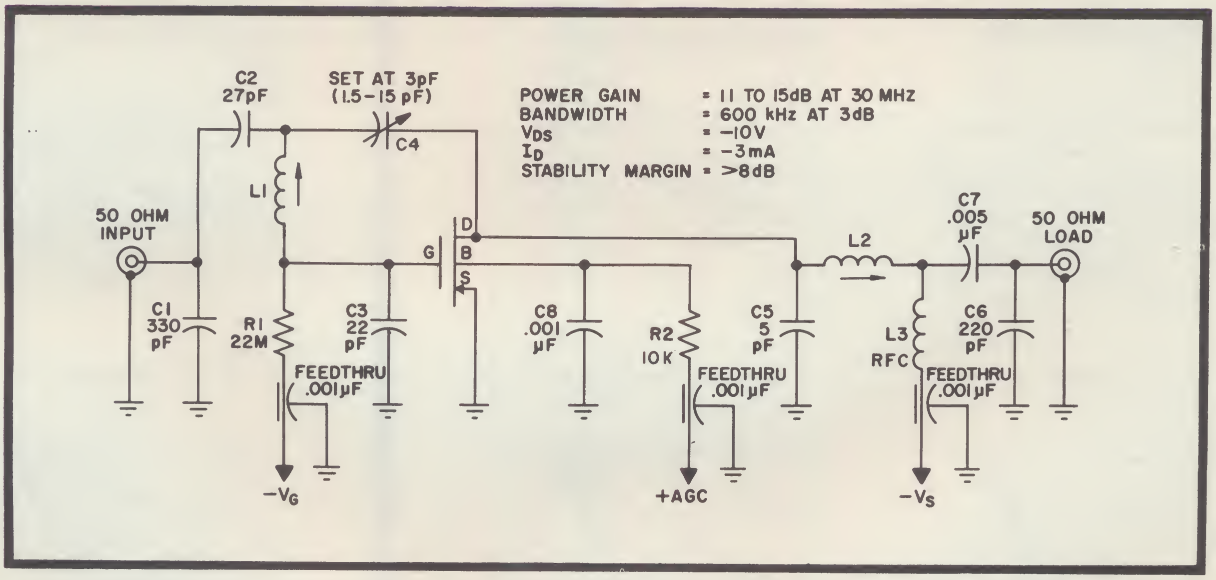


DYNAMIC DRAIN RESISTANCE VS TEMPERATURE



APPLICATIONS

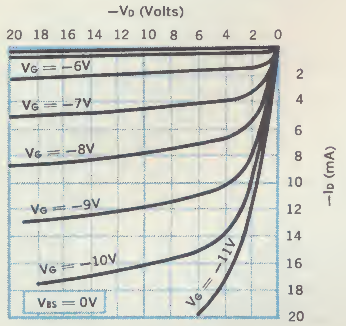
30 MHz Amplifier Utilizing a 2N4353



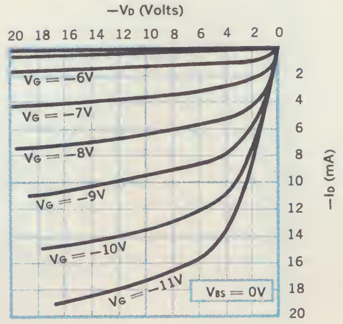
TYPICAL CHARACTERISTIC CURVES

All curves have been plotted from photographs taken with a Tektronix Curve Tracer, Model 575

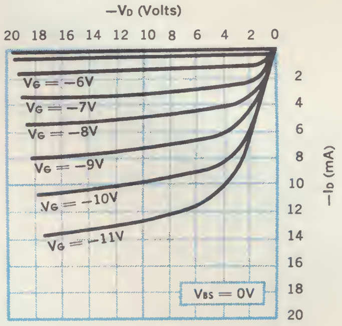
DRAIN CHARACTERISTICS AT –55°C



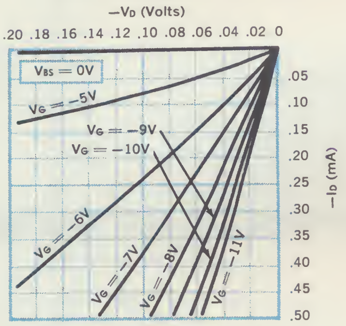
DRAIN CHARACTERISTICS AT 25°C



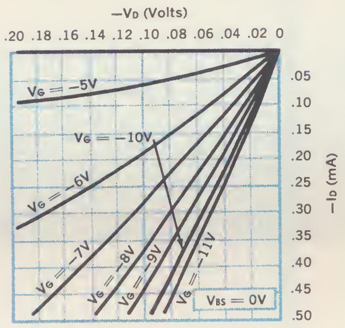
DRAIN CHARACTERISTICS AT 125°C



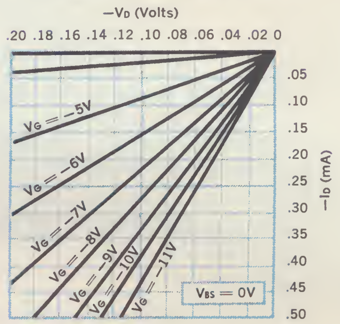
DRAIN CHARACTERISTICS AT –55°C



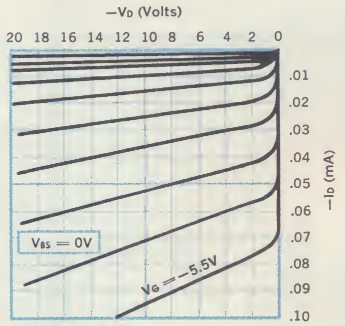
DRAIN CHARACTERISTICS AT 25°C



DRAIN CHARACTERISTICS AT 125°C

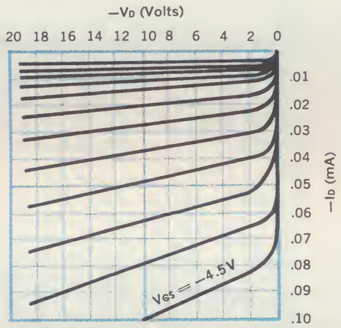


DRAIN CHARACTERISTICS AT –55°C



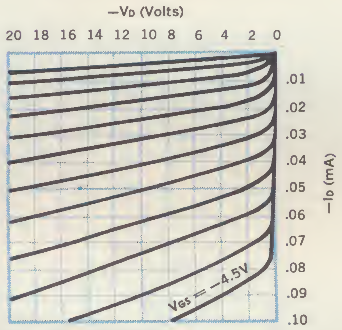
VG in .05 V Steps

DRAIN CHARACTERISTICS AT 25°C



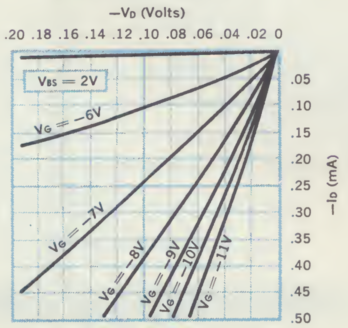
VBS = 0V, .05 V Steps

DRAIN CHARACTERISTICS AT 125°C

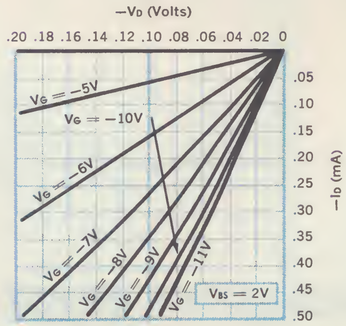


VBS = 0V, .05 V Steps

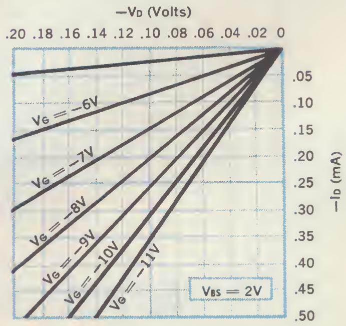
DRAIN CHARACTERISTICS AT –55°C



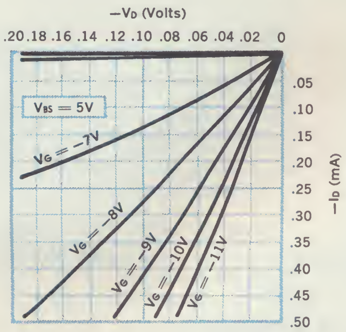
DRAIN CHARACTERISTICS AT 25°C



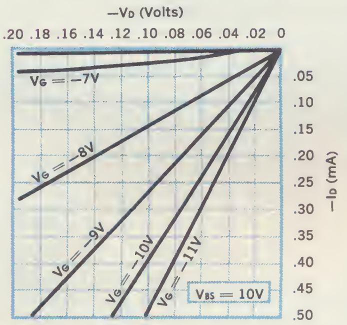
DRAIN CHARACTERISTICS AT 125°C



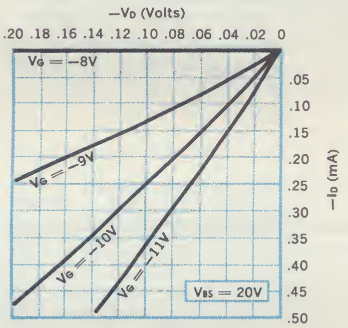
DRAIN CHARACTERISTICS AT −55°C



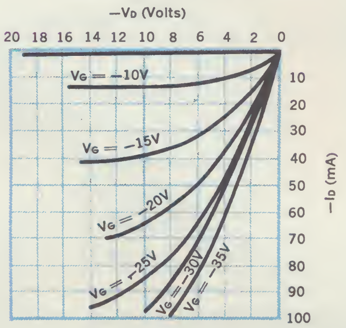
DRAIN CHARACTERISTICS AT −55°C



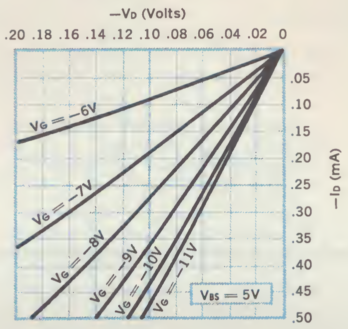
DRAIN CHARACTERISTICS AT −55°C



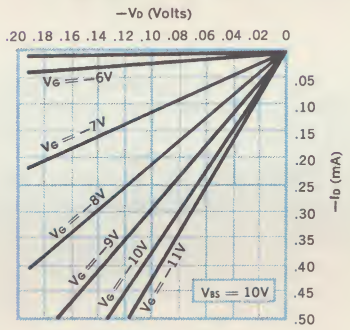
DRAIN CHARACTERISTICS AT 25°C



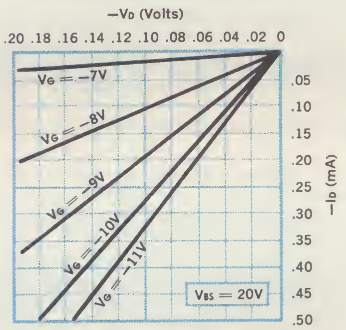
DRAIN CHARACTERISTICS AT 25°C



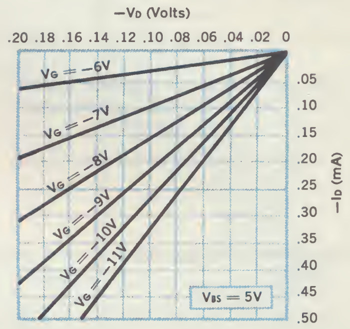
DRAIN CHARACTERISTICS AT 25°C



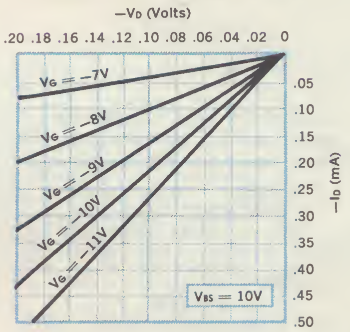
DRAIN CHARACTERISTICS AT 25°C



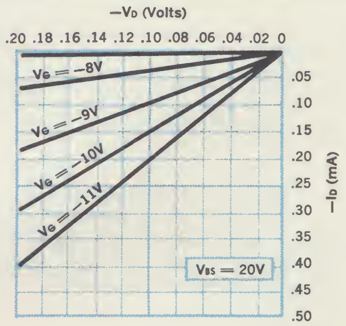
DRAIN CHARACTERISTICS AT 125°C



DRAIN CHARACTERISTICS AT 125°C



DRAIN CHARACTERISTICS AT 125°C



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